In the Claims:

Please amend the Claims as follows:

1. - 2. (Canceled)

3. (Previously presented) A liquid crystal display comprising:

a liquid crystal panel assembly including a first, a second and a third scanning area, each of the scanning areas including a plurality of gate lines connected to a plurality of pixels which include switching elements connected to the gate lines and data lines;

a gate driver applying a voltage to the gate lines for turning on the switching elements;

a data driver selecting gray voltages corresponding to gray signals and applying the selected gray voltages to the pixels via the data lines as data signals, each of the data signals including normal data signals and a black data signal; and

a signal controller providing the gray signals and control signals for controlling the gate driver and the data driver, wherein, in one frame period, the signal controller controls the gate driver and the data driver such that the black data signal is applied to pixels connected to gate lines of the second scanning area while gate-on voltages are applied to the gate lines of the second scanning area and then, the normal data signals are applied to pixels connected

to gate lines of the first scanning area while gate-on voltages are sequentially applied to the gate lines of the first scanning area in an arranging direction in which the gate lines are arranged;

the signal controller controls the gate driver and the data driver such that, in said one frame period, gate-on voltages are applied to gate lines of the third scanning area after the gate-on voltage is applied to the last gate line of the first scanning area and then the black data signal is applied to pixels connected to the gate lines of the third scanning area,

wherein, in a frame period next to said one frame period, the signal controller controls the gate driver and the data driver such that the black data signal is applied to pixels connected to gate lines of the second scanning area while gate-on voltages are applied to the gate lines of the second scanning area and then, the normal data signals are applied to the pixels connected to gate lines of the first scanning area while gate-on voltages are sequentially applied to the gate lines of the first scanning area in a direction opposite to the arranging direction of the gate lines.

4. (Original) The liquid crystal display of claim 3, wherein the black data signal is simultaneously applied to the pixels in one of the scanning areas.

5. (Previously presented) The liquid crystal display of claim 3, wherein, while gate-on voltages are applied to one of the scanning areas, pixels connected to gate lines of the other of the scanning areas hold previous data

signals.

6. (Canceled)

7. (Previously presented) The liquid crystal display of claim 3, wherein the liquid crystal display is in an optically compensated bend mode.

8. - 19. (Canceled)

20. (Previously presented) The liquid crystal display of claim 3, wherein, in the frame period next to said one frame period,

the signal controller controls the gate driver and the data driver such that gate-on voltages are applied to gate lines of the third scanning area after the gate-on voltage is applied to the last gate line of the first scanning area and then the black data signal is applied to the pixels connected to the gate lines of the third scanning area in the frame period next to said one frame period.

21. (Previously presented) The liquid crystal display of claim 20, wherein polarity of voltages of the normal data signals applied in said one frame period is opposite to polarity of the normal data voltages applied in the frame period next to said one frame period.

22. (Previously presented) The liquid crystal display of claim 20, wherein

polarity of a voltage of the black data signal applied in said one frame period is opposite to polarity of a voltage of the black data signal applied in the frame period next to said one frame period.

23. (Previously presented) The liquid crystal display of claim 20, wherein a holding period, in which the pixels hold the normal data signals, averaged over two adjacent frames is uniform.

24. (Previously presented) The liquid crystal display of claim 3, wherein pixels connected to one of the gate lines are arranged in a direction perpendicular to the arranging direction of the gate lines.

25. (Previously presented) The liquid crystal display of claim 3, wherein

the gate driver includes a plurality of gate driving devices;

the gate driving devices are connected to the gate lines; and

the pixels are connected to the gate driving devices through the gate lines, respectively.

26. (Previously presented) The liquid crystal display of claim 3, wherein the signal controller further controls the gate driver and the data driver such that equal to or more than 50% of the pixels in the scanning areas hold the black data signal.

27. (Previously presented) The liquid crystal display of claim 3, wherein, in said one frame period, the signal controller further controls the gate driver and the data driver such that the normal data signals are applied to the pixels connected to gate lines of the second scanning area after the black data signal is applied to pixels connected to the gate lines of the third scanning area.

28. (Previously presented) A method of driving a liquid crystal panel assembly including

a first, a second and a third scanning area, each of the scanning areas including a plurality of gate lines connected to a plurality of pixels which includes switching elements connected to the gate lines and data lines; a gate driver applying a voltage to the gate lines for turning on the switching elements; a data driver selecting gray voltages corresponding to gray signals and applying the selected gray voltages to the pixels via the data lines as data signals, each of the data signals including normal data signals and a black data signal; and a signal controller providing the gray signals and control signals for controlling the gate driver and the data driver, the method comprising:

applying, in one frame period, the black data signal to pixels connected to gate lines of the second scanning area while gate-on voltages are applied to the gate lines of the second scanning area;

then, applying, in said one frame period, the normal data signals to the pixels connected to gate lines of the first scanning area while gate-on voltages are sequentially applied to the gate lines of the first scanning area in an

arranging direction in which the gate lines are arranged;

applying, in said one frame period, gate-on voltages to gate lines of the third scanning area after the gate-on voltage is applied to the last gate line of the first scanning area;

applying the black data signal to the pixels connected to the gate lines of the third scanning area in said one frame period,

applying, in a frame period next to said one frame period, the black data signal to pixels connected to gate lines of the second scanning area while gate-on voltages are applied to the gate lines of the second scanning area; and

then, applying, in the frame period next to said one frame period, the normal data signals to the pixels connected to gate lines of the first scanning area while gate-on voltages are sequentially applied to the gate lines of the first scanning area in a direction opposite to the arranging direction of the gate lines.

29. (Previously presented) The method of claim 28, further comprising:

after applying, in the frame period next to said one frame period, the normal data signals to the pixels in the first scanning area,

then applying gate-on voltages to gate lines of the third scanning area after the gate-on voltage is applied to the last gate line of the first scanning area and applying the black data signal to the pixels connected to the gate lines of the third scanning area in the frame period next to said one frame period.

30. (Previously presented) The method of claim 29, wherein polarity of

voltages of the normal data signals applied in said one frame period is opposite to polarity of the normal data voltages applied in the frame period next to said one frame period.

31. (Previously presented) The method of claim 29, wherein polarity of a voltage of the black data signal applied in said one frame period is opposite to polarity of a voltage of the black data signal applied in the frame period next to said one frame period.

32. (Previously presented) The method of claim 28, wherein equal to or more than 50% of the pixels in the scanning areas hold the black data signal.

33. (Previously presented) The method of claim 28, further comprising, applying the normal data signals to the pixels connected to gate lines of the second scanning area in said one frame period after the black data signal is applied to pixels connected to the gate lines of the third scanning area.

34. (Currently amended) A liquid crystal display comprising:

a liquid crystal panel assembly including M scanning areas, wherein M is an integer greater than 2, each of the scanning areas including a plurality of gate lines connected to a plurality of pixels which include switching elements connected to the gate lines and data lines;

a gate driver applying a voltage to the gate lines for turning on the

switching elements;

a data driver selecting gray voltages corresponding to gray signals and applying the selected gray voltages to the pixels via the data lines as data signals, each of the data signals including normal data signals and a black data signal, wherein each scanning area is applied with normal data signals during normal data signal driving time corresponding to each scanning area, and wherein each scanning area is applied with black data signals during black data signal driving time corresponding to each scanning area; and

a signal controller providing the gray signals and control signals for controlling the gate driver and the data driver, wherein, in one frame period,

the signal controller controls the gate driver and the data driver such that the normal data signals are applied to pixels connected to gate lines of the N-th scanning area while gate-on voltages are sequentially applied to the gate lines of the N-th scanning area in an arranging direction in which the gate lines are arranged during normal data signal driving time, wherein N is an integer equal to or less than M;

the signal controller controls the gate driver and the data driver such that, in said one frame period, the black data signal is applied to pixels connected to gate lines of the N-th scanning area while gate-on voltages are applied to the gate lines of the N-th scanning area during black data signal driving time;

wherein, in a frame period next to said one frame period, the signal controller controls the gate driver and the data driver such that the normal data signals are applied to pixels connected to gate lines of the N-th scanning area

while gate-on voltages are sequentially applied to the gate lines of the N-th scanning area in a direction opposite to the arranging direction ~~of~~ in which the gate lines are arranged during normal data signal driving time and, the black data signal is applied to pixels connected to gate lines of the N-th scanning area while gate-on voltages are applied to the gate lines of the second scanning area during black data signal driving time, and

wherein in one frame, at least one of the M scanning areas displays a corresponding gray by the applied normal data signals, and the at least one of the M scanning areas displays a corresponding black gray by the applied black data signals.